REMARKS

Claims 109-112, 115, 116, 119, 120, 123, 127 and 129-135 are pending. Claims 87-90, 117, 118, 121, 122, 124-126 and 128 are cancelled without prejudice or disclaimer, claims 109-112, 115, 119, 123 and 127 are amended, and new claims 132-135 are added. A marked-up version showing the changes made by the present amendment is attached hereto as "Version with markings to show changes made".

The rejection of claims 121 and 122 under 35 USC §112, first paragraph, is rendered moot by cancellation of these claims.

Claims 117-120 were rejected under 35 USC §112, second paragraph, as being indefinite. It is respectfully submitted that the presently amended claims are in full compliance with 35 USC §112.

The rejection of claims 87-90 under 35 USC §102(e) as being anticipated by Kata has been rendered moot by cancellation of these claims.

Claims 109-112 and 131 were rejected under 35 USC §102(e) as being anticipated by Yasunaga. Favorable reconsideration of this rejection is requested in view of the amendments made herein.

Independent claims 109 and 111 have been amended to clarify that (a) the external connection protruding electrodes form a bump, and (b) the bump has a height larger than a height of the protruding electrode for a part thereof protruding beyond the resin layer. See Fig. 39A.

It is noted that the solder 115 of Yasunaga illustrated in Fig. 101A is merely a solder layer plated on the surface of the protruded electrode 112. With such a thin solder layer, it is not possible

to achieve stress relaxation.

With respect to claims 110 and 112, the Examiner argues that Yasunaga inherently has the structural feature of theses claims. It is respectfully submitted that the Examiner is incorrect.

Claims 110 and 112 have the feature that both the resin layer and the semiconductor device have a surface formed by cutting made by a dicer. Yasunaga lacks such a surface. The surface of Yasunaga is formed as a result of a molding process. Thus, in order to highlight this difference, claims 110 and 112 specify that "both of a side portion of the resin layer and a side portion of the semiconductor element are respectively exposed".

Claims 115-120 were rejected under 35 USC §102(b) as being anticipated by Matsubara. Favorable reconsideration of this rejection is requested in view of the amendments made herein.

Claims 117 and 118 have been cancelled. Furthermore, claims 115 and 119 have been amended based on Figs. 39A and 39B. More specifically, amended claims 115 and 119 set forth that the protruding electrodes are formed on respective lead lines. Thus, the external stress applied to the protruding electrodes at the time of mounting of the semiconductor device is dispersed via the lead lines. As such, concentration of stress to the protruding electrode is avoided. Furthermore, the structure is effective for dispersing the stress applied to the protruding electrodes at the time of compression molding of the resin layer so that it becomes possible to use a higher compression at the time of the molding process. As a result, reliability of the resin layer is increased. Accordingly, the amended claims distinguish over the cited reference.

Claims 121-123 were rejected under 35 USC §102(e) as being anticipated by Brooks. It is believed that this rejection has been rendered moot by cancellation of claims 121 and 122, and

amendment of claim 123 to depend from claim 127.

Claims 124-130 were rejected under 35 USC §102(b) as being anticipated by Nishino. Favorable reconsideration of this rejection is earnestly solicited.

Claims 124-126 and 128 have been cancelled. Claim 127 has been amended to incorporate the features of claim 128, in order to clarify that the semiconductor device is formed by wafer-level packaging technology.

It is noted that the Examiner considers the protrusion electrodes 5 as corresponding to both the claimed protruding electrode and the protrusion for positioning of the semiconductor device. Furthermore, on page 12 of the Office Action, the Examiner argues that the claims set forth an intended use.

It is very clear that the physical property of the "compression-molded layer" used in the present invention is different from that of the resin layer of Nishino, in which the resin layer is formed by a spin-coating process or squeeze printing process. Table I of IEEE Transactions on Advanced Packaging, which was submitted with the response filed on January 18, 2002, compares the property of the resin layer formed by a dispensing process and the resin layer formed by the transfer molding process, for the case of a DIP type package.

Here, the dispensing process is a process conducted by holding a molten resin in a vessel like a syringe and achieving resin sealing by dripping the resin. Thus, the resin layer formed by the dispensing process is free from compression at the time of the resin formation.

Contrary to the dispensing process, the transfer molding process pushes a molten resin into a mold and the resin layer is formed under pressure exerted at the time of the resin injection. As is

clearly seen in the foregoing article, a resin layer of higher reliability is obtained by using the transfer molding process. As noted in the article, the reason of this improvement is caused a s a result of curing of the resin under high pressure and associated high adherence between the resin layer and the underlying layer.

Thus, the resin layer formed under pressure is distinct over the resin layer formed without pressure.

As noted previously, Nishino merely teaches a spin-coating process and a squeeze printing process for the resin formation process. The process of Nishino does not use pressure at the time of resin formation, and only poor reliability is achieved. The resin layer of Nishino is clearly distinct and is distinguishable over the resin of the present invention.

Meanwhile, the IEEE article also describes that, while it is possible to form a resin layer of high-reliability by transfer molding process at the time of sealing a chip, such a process cannot be used for a wafer and that it is necessary to use a compressional molding process when sealing a wafer with a resin layer under pressure.

New claims 132-135 have been added. New claim 132 corresponds to claim 42, which had been inadvertently cancelled. New claim 132 distinguishes over the cited art, particularly Kata, in the point that the devices of Kata have the feature of a terminal side and a rear side of the chip, both sealed with a resin layer (see Fig. 4 and Figs. 20A-20C of Kata) which are formed by a process other than the wafer-level packaging. Thus, the device of Kata inherently lacks the feature of new claim 132.

For at least the foregoing reasons, the claimed invention distinguishes over the cited art and

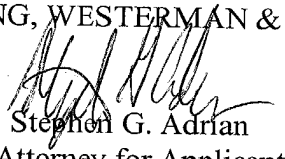
defines patentable subject matter. Favorable reconsideration is earnestly solicited.

Should the Examiner deem that any further action by Applicants would be desirable to place the application in condition for allowance, the Examiner is encouraged to telephone Applicants' assigned attorney.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP



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Enclosures: Version with markings to show changes made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE 09/029,608

IN THE CLAIMS:

Please amend the claims as follows:

109. (Twice Amended) A semiconductor device comprising:

a semiconductor element having a surface on which protruding electrodes are formed;

a resin layer formed on the surface of the semiconductor element so as to seal the protruding electrodes except end portions thereof; and

external connection protruding electrodes provided to the end portions of the protruding electrodes that protrude from the resin layer,

said external connection protruding electrodes forming a bump,

said bump having a height larger than a height of said protruding electrode for a part thereof protruding beyond said resin layer.

110. (Twice Amended)The semiconductor device as claimed in claim 109, wherein both a side portion of the resin layer and a side portion of the semiconductor element [have surfaces defined by cutting using a dicer] are respectively exposed.

111. (Twice Amended) A semiconductor device comprising:

a semiconductor element having a surface on which protruding electrodes having convex end portions are formed;

a resin layer formed on the surface of the semiconductor element so as to seal the protruding electrodes except the convex end portions thereof; and

external connection protruding electrodes provided to the convex end portions of the protruding electrodes that protrude from the resin layer,

said external connection protruding electrodes forming a bump,

said bump having a height larger than a height of said protruding electrode for a part thereof protruding beyond said resin layer.

112. (Amended) The semiconductor device as claimed in claim 111, wherein both of a side portion of the resin layer and a side portion of the semiconductor element [have surfaces defined by cutting using a dicer] are respectively exposed.

115. (Twice Amended) A semiconductor device comprising :

a semiconductor element having a surface on which electrode pads connected to an internal part of the semiconductor element and protruding electrodes to be connected to an external part are formed; [and]

lead lines each connecting one of the electrode pads and one of the protruding electrodes so that the protruding electrodes and the internal pad are connected through the lead lines; and

a resin layer formed on the surface of the semiconductor element so as to seal the protruding electrodes except end portions thereof,

the protruding electrodes having a core portion and an electrically conductive film formed

on a surface of the [protruding] core portion,

the core portions of the protruding electrodes are directly formed on the lead lines,

wherein the core portion comprises an elastic resin.

119. (Twice Amended) A semiconductor device comprising:

a semiconductor element having a surface on which electrode pads connected to an internal part of the semiconductor element and protruding electrodes to be connected to an external part are formed;

lead lines each connecting one of the electrode pads and one of the protruding electrodes so that the protruding electrodes and the internal part are connected through the lead lines;

a resin layer formed on the surface of the semiconductor element so as to seal the protruding electrodes except end portions thereof; and

external connection protruding electrodes provided to the end portions of the protruding electrodes that protrude from the resin layer,

the protruding electrodes having a core portion and an electrically conductive film formed on a surface of the [protruding] core portion,

the core portions of the protruding electrodes are directly formed on the lead lines,

wherein the core portion comprises an elastic resin.

123. (Twice Amended) A semiconductor device as claimed in claim 127 [comprising:

a semiconductor element having a surface on which protruding electrodes are formed;

and

a resin layer formed on the surface of the semiconductor element so as to seal the protruding electrodes except end portions thereof,]

wherein a part of a side portion of the semiconductor element being covered with the resin layer,

a part of a side portion of said semiconductor elements being exposed.

127. (Amended) A semiconductor device comprising:

a semiconductor element having a surface on which protruding electrodes are formed; and

a compression-molded resin layer formed on the surface of the semiconductor element so as to seal the protruding electrodes except end portions thereof,

wherein the compression-molded resin layer and the semiconductor element have surfaces defined by cutting using a dicer.